CLAIMS

1. A microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor.

2. The microcomputer according to claim 1, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

3. The microcomputer according to claim 2, wherein the processor is further configured transmit to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

4. The microcomputer according to claim 3, wherein the processor is further configured transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

5. The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a value indicating an increment of the program counter of the processor.

6. The microcomputer according to claim 1, wherein the processor is further configured to transmit to the debug circuit a process identifier value.

7. The microcomputer according to claim 1, wherein the processor is further configured to transmit to the debug circuit an signal indicating that a current process identifier value differs from a processor identifier value of a previously-executed instruction.

8. The microcomputer according to claim 1, wherein the debug circuit is configured to store the program counter of the processor in a memory-mapped register.

9. The microcomputer according to claim 1, wherein the debug circuit is adapted to generate trace information including the program counter.

10. The microcomputer according to claim 1, wherein the microcomputer is implemented on a same integrated circuit.

11. The microcomputer according to claim 5, wherein the processor is further configured to transmit to the debug circuit a value indicating an amount by which program counter is incremented.

12. A microcomputer comprising:

at lease one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

13. The microcomputer according to claim 12, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

14. The microcomputer according to claim 13, wherein the processor includes means for transmitting to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

15. The microcomputer according to claim 14, wherein the processor includes means for transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

16. The microcomputer according to claim 12, wherein the processor includes means for transmitting to the debug circuit a value indicating an increment of the program counter of the processor.

17. The microcomputer according to claim 12, wherein the processor includes means for transmitting to the debug circuit a process identifier value.

18. The microcomputer according to claim 12, wherein the processor includes means for transmitting to the debug circuit an signal indicating that a current process identifier value differs from a processor identifier value of a previously-executed instruction.

19. The microcomputer according to claim 12, wherein the debug circuit includes means for storing the program counter of the processor in a memory-mapped register.

20. The microcomputer according to claim 12, wherein the debug circuit includes means for generating trace information including the program counter.

21. The microcomputer according to claim 12, wherein the microcomputer is implemented on a same integrated circuit.

22. The microcomputer according to claim 16, wherein the processor includes means for transmitting to the debug circuit a value indicating an amount by which the program counter is incremented.

23. A method for transferring information between a processor and a debug circuit of a microcomputer, the method comprising steps of:

transmitting to the debug circuit a program counter value indicating the program counter of the processor.

24. The method according to claim 23, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

25. The method according to claim 23, the method further comprising a step of transmitting to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

26. The method according to claim 25, the method further comprising a step of transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

27. The method according to claim 23, the method further comprising a step of transmitting to the debug circuit a value indicating an increment of the program counter of the processor.

28. The method according to claim 23, the method further comprising a step of transmitting to the debug circuit a process identifier value.

29. The method according to claim 23, the method further comprising a step of transmitting to the debug circuit an signal indicating that a current process identifier value differs from a processor identifier value of a previously-executed instruction.

30. The method according to claim 23, the method further comprising a step of storing the program counter of the processor in a memory-mapped register of the debug circuit.

31. The method according to claim 23, the method further comprising a step of generating trace information including the program counter.

32. The method according to claim 23, wherein the microcomputer is implemented on a same integrated circuit.

33. The method according to claim 27, further comprising a step of incrementing the program counter by a value depending upon a mode signal.